AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor device, comprising: a plurality of wiring layers that are laminated with each other,

each of said wiring layers ~~includes~~comprising:

an interlayer insulating film;

first and second electrodes buried in the interlayer insulating film and remote from each other;

a first via that connects ~~said~~ the first electrode of one wiring layer ~~and~~ to the~~said~~ first electrode of ~~the~~ an adjacent wiring layer~~, which is provided on its upper layer or lower layer, to each other~~; and

a second via that connects ~~said~~ the second electrode of one wiring layer to the ~~and said~~ second electrode of ~~the~~ an adjacent wiring layer, ~~which is provided on its upper layer or lower layer, to each other,~~ and said connected first electrodes and said first via are connected to a first terminal, said connected second electrodes and said second via are connected to a second terminal, and a capacitor is formed between said first electrodes and said first via connected to said first terminal~~,~~ and said second electrodes and said second via connected to said second terminal; and

wherein said semiconductor device further comprises an integrated circuit section, wherein the diameter of said first and second via are larger than the diameter of via provided in said integrated circuit section.

2. (currently amended): The semiconductor device according to Claim 1, wherein a plurality of said wiring layers follow the ~~are provided in a~~ same design rule ~~with each other.~~; and

said design rule comprises said first and second electrodes having widths in a first predetermined range, the distance between said first electrode and said second electrode in the same wiring layer being in a second predetermined range, and the distance between said first via and said second via that is formed in the closest position to the first via being in a third predetermined range.

3. (currently amended): The semiconductor device according to Claim 1, wherein said plurality of wiring layers comprises at least ~~are provided in~~ three ~~or more~~ layers.

4. (currently amended): The semiconductor device according to Claim 3, wherein a plurality of said first via are arranged in a position where the first via overlap with each other and a plurality of said second via are arranged in a position where the second via overlap with each other, viewing from the lamination direction of said wiring layers.

5. (currently amended): The semiconductor device according to Claim 1, wherein a plurality of said first electrodes are arranged in a position whereby the first electrodes overlap with each other and a plurality of said second electrodes are arranged in a position whereby the second electrodes overlap with each other, viewing from the lamination direction of said wiring layers.

6. (currently amended): The semiconductor device according to Claim 1, wherein the distance between said first electrode and said second electrode is 0.3μm or less in ~~a same~~ the same wiring layer.

7. (currently amended): The semiconductor device according to ~~Claim 1~~ Claim 2, wherein the distance between said first electrode and said second electrode in ~~a same~~the same wiring layer is the minimum value ~~that is allowed by the design rule of said wiring layer~~of said second predetermined range.

8. (currently amended): The semiconductor device according to Claim 1, wherein the distance between said first via and said second via that is formed in the closest position to the first via is the minimum value of said third predetermined range. ~~that is allowed by the design rule of said wiring layer.~~

9. (original): The semiconductor device according to Claim 1, wherein said first and second electrodes are in strip shapes that are parallel to each other.

10. (original): The semiconductor device according to Claim 9, wherein the width of said first and second electrodes is 0.3μm or less.

11. (currently amended): The semiconductor device according to Claim 2~~9~~, wherein said first and second electrodes are in strip shapes parallel to each other; and

wherein the width of said first and second electrodes is the minimum value of said first predetermined range.~~allowed by the design rule of said wiring layers.~~

12. (original): The semiconductor device according to Claim 9, wherein said first and second electrodes are provided in each of said wiring layers in plural numbers, and said first and second electrodes are arrayed alternately in each wiring layer.

13. (currently amended): The semiconductor device according to Claim 9, wherein ~~regarding each of said first and second electrodes,~~ said first and second via are provided in plural numbers ~~by being arrayed in~~ the longitudinal direction of said first and second electrodes.

14. (currently amended): A semiconductor device, comprising: a plurality of wiring layers that are laminated with each other,

each of said wiring layers comprising:

an interlayer insulating film;

first and second electrodes buried in the interlayer insulating film and remote from each other;

a first via that connects the first electrode of one wiring layer to the first electrode of an adjacent wiring layer; and

a second via that connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer, and said connected first electrodes and said first via are connected to a first terminal, said connected second electrodes and said second via are connected to a second terminal, and a capacitor is formed between said first electrodes and said first via connected to said first terminal and said second electrodes and said second via connected to said second terminal;

wherein said first and second electrodes are in strip shapes that are parallel to each other;

wherein said first and second via are provided in plural numbers in the longitudinal direction of said first and second electrodes; and

~~The semiconductor device according to Claim 13~~, wherein the distance between said first via in the longitudinal direction of said first electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers, and the distance between said second via in the longitudinal direction of said second electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers.

15. (original): The semiconductor device according to Claim 9, wherein at least one of said first and second via is a slit-shaped via extending in the longitudinal direction of said first and second electrodes.

16. (canceled).

17. (currently amended): A semiconductor device, comprising: a plurality of wiring layers that are laminated with each other,

each of said wiring layers comprising:

an interlayer insulating film;

first and second electrodes buried in the interlayer insulating film and remote from each other;

a first via that connects the first electrode of one wiring layer to the first electrode of an adjacent wiring layer; and

a second via that connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer, and said connected first electrodes and said first via are connected to a first terminal, said connected second electrodes and said second via are connected to a second terminal, and a capacitor is formed between said first electrodes and said first via connected to said first terminal and said second electrodes and said second via connected to said second terminal;

~~The semiconductor device according to Claim 1,~~ wherein said first terminal is connected to ground wiring and~~,~~ said second terminal is connected to power source wiring.~~, and said capacitor is a decoupling capacitor connected to a power source in parallel.~~

18. (original): The semiconductor device according to Claim 17, wherein said wiring layers are formed in a semiconductor chip, and said ground wiring and said power source wiring are arranged in the periphery of said semiconductor chip.

19. (currently amended): A semiconductor device, comprising: a plurality of wiring layers that are laminated with each other,

each of said wiring layers comprising:

an interlayer insulating film;

first and second electrodes buried in the interlayer insulating film and remote from each other;

a first via that connects the first electrode of one wiring layer to the first electrode of an adjacent wiring layer;

a second via that connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer, and said connected first electrodes and said first via are connected to a first terminal, said connected second electrodes and said second via are connected to a second terminal, and a capacitor is formed between said first electrodes and said first via

connected to said first terminal and said second electrodes and said second via connected to said second terminal;~~The semiconductor device according to Claim 1, further comprising:~~

wherein said semiconductor device further comprises: an upper electrode provided in a region including a region immediately under said first and second electrodes, and said upper electrode being connected to one of said first and second terminals;

an insulating film provided under the upper electrode; and

a lower electrode provided under the insulating film and connected to the other one of said first and second terminals, wherein another capacitor is formed between said upper electrode and said lower electrode.

20. (currently amended): A semiconductor device, comprising: a plurality of wiring layers that are laminated with each other,

each of said wiring layers comprising:

an interlayer insulating film;

first and second electrodes buried in the interlayer insulating film and remote from each other;

a first via that connects the first electrode of one wiring layer to the first electrode of an adjacent wiring layer;

a second via that connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer, and said connected first electrodes and said first via are connected to a first terminal, said connected second electrodes and said second via are connected

to a second terminal, and a capacitor is formed between said first electrodes and said first via connected to said first terminal and said second electrodes and said second via connected to said second terminal;~~The semiconductor device according to Claim 1, further comprising:~~

wherein said semiconductor device further comprises: an N-type semiconductor layer, which is provided in a region including a region immediately under said first and second electrodes, said N-type semiconductor layer being ~~and~~ connected to one terminal out of said first and second terminals, to which a higher potential is applied; and

a P-type semiconductor layer, which is provided in a region including the region immediately under ~~the~~ said first and second electrodes so as to contact said N-type semiconductor layer and connected to the other one terminal out of said first and second terminals, to which a lower potential is applied, wherein

~~still~~ another capacitor is formed between said N-type semiconductor layer and said P-type semiconductor layer.

21. (currently amended): A semiconductor device, comprising: a plurality of wiring layers that are laminated with each other,

each of said wiring layers comprising:

an interlayer insulating film;

first and second electrodes buried in the interlayer insulating film and remote from each other;

a first via that connects the first electrode of one wiring layer to the first electrode of an adjacent wiring layer;

a second via that connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer, and said connected first electrodes and said first via are connected to a first terminal, said connected second electrodes and said second via are connected to a second terminal, and a capacitor is formed between said first electrodes and said first via connected to said first terminal and said second electrodes and said second via connected to said second terminal;~~The semiconductor device according to Claim 1, further comprising~~

wherein said semiconductor device further comprises a semiconductor substrate provided under said wiring layers, and wherein the semiconductor substrate ~~includes~~comprises:

an N-type semiconductor region, which is provided in a region including a region immediately under said first and second electrodes and connected to one terminal out of said first and second terminals, to which higher potential is applied; and

a P-type semiconductor region, which is provided in a region including the region immediately under ~~the~~ said first and second electrodes so as to contact said N-type semiconductor region and connected to the other one terminal out of said first and second terminals, to which lower potential is applied, and ~~still~~ another capacitor is formed between said N-type semiconductor region and said P-type semiconductor region.